source supplying a current to the summing node; and

an indicator circuit having an input connected to the summing node, wherein the indicator circuit is responsive to changes in the summing node voltage level and generates at an output a logical signal at one state when the summing node voltage level is greater than the predetermined threshold voltage level and generates the logical signal at the output at another state when the summing node voltage level is less than the predetermined threshold voltage level.

Please add the following new claims:

--31. A direct current sum bandgap voltage comparator comprising:

a summing node;

first and second current sources connected between the summing node and a lower power supply; and

third and fourth current sources connected between the summing node and an upper power supply,

wherein a voltage at the summing node equals a voltage of the upper power supply when a current from the first and second current sources to the summing node exceeds a current from the third and fourth current sources to the summing node, and

wherein the voltage at the summing node equals a voltage of the lower power supply when the current from the third and fourth current sources to the summing node exceeds the current from the first and second current sources to the summing node.

32. The direct current sum bandgap voltage comparator of claim 31, wherein the first current source further comprises:

a first field effect transistor connected between the lower power supply and the summing node;

a second field effect transistor connected at a source to the lower power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor;

a third field effect transistor connected at a source to the

lower power supply and connected at a gate to the gate of the first field effect transistor;

a fourth field effect transistors connected at a drain to the drain of the second field effect transistor;

a fifth field effect transistor connected at a drain to a drain of the third field effect transistor and to a gate of the fifth field effect transistor and connected at the gate to a gate of the fourth field effect transistor;

a first bipolar junction transistor connected at a base and a collector to the upper power supply;

a second bipolar junction transistor connected at a base and a collector to the upper power supply and connected at an emitter to a source of the fifth field effect transistor; and

a resistor connected to an emitter of the first bipolar junction transistor and to a source of the fourth field effect transistor.

33. The direct current sum bandgap voltage comparator of claim 32, wherein the first, second, and third field effect transistors are n-channel MOSFETs and the fourth and fifth field effect transistors are p-channel MOSFETs.

34. The direct current sum bandgap voltage comparator of claim 32, wherein the first field effect transistor is sized to generate a current of N times a current flowing through the second field effect transistor.

35. The direct current sum bandgap voltage comparator of claim 31, wherein the first current source further comprises:

a current mirror including a field effect transistor connected between the lower power supply and the summing node, wherein the field effect transistor is sized to generate a current of N times a current flowing through a portion of the current mirror.

36. The direct current sum bandgap voltage comparator of claim 31, wherein the second current source further comprises:

a first field effect transistor connected between the lower power supply and the summing node;

a second field effect transistor connected at a source to the lower power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor;

a third field effect transistor connected at a source to the lower power supply and connected at a gate to the gate of the first field effect transistor;

a fourth field effect transistor connected at a drain to the drain of the second field effect transistor;

a fifth field effect transistor connected at a drain to a drain of the third field effect transistor and to a gate of the fifth field effect transistor and connected at the gate to a gate of the fourth field effect transistor;

a bipolar junction transistor connected at a base and a collector to the upper power supply and at an emitter to the source of the fifth field effect transistor; and

a resistor connected between a source of the fourth field effect transistor and the upper power supply.

37. The direct current sum bandgap voltage comparator of claim 36, wherein the first, second, and third field effect transistors are n-channel MOSFETs and the fourth and fifth field effect transistors are p-channel MOSFETs.

38. The direct current sum bandgap voltage comparator of claim 31, wherein the third current source further comprises:

a first field effect transistor connected between the upper power supply and the summing node;

a second field effect transistor connected at a source to the upper power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor;

a third field effect transistor connected at a source to the lower power supply and connected at a drain to the drain of the second field effect transistor;

a fourth field effect transistor connected at a source to the lower power supply, at a gate to a gate of the third field effect transistor, and at a drain to the gate of the fourth field effect transistor;

a fifth field effect transistor connected at a source to the lower power supply;

a sixth field effect transistor connected at a drain to the drain of the fourth field effect transistor;

a seventh field effect transistor connected at a drain to a drain of the fifth field effect transistor and to a gate of the seventh field effect transistor and connected at the gate to a gate of the sixth field effect transistor;

an eighth field effect transistor connected at a drain and at a gate to a source of the seventh field effect transistor and at a source to the upper power supply; and

a resistor connected between a source of the sixth field effect transistor and the upper power supply.

39. The direct current sum bandgap voltage comparator of claim 38, wherein the first, second, sixth, seventh, and eighth field effect transistors are p-channel MOSFETs and the third, fourth and fifth field effect transistors are n-channel MOSFETs.

40. The direct current sum bandgap voltage comparator of claim 31, wherein the fourth current source further comprises:

a first field effect transistor connected between the upper power supply and the summing node;

a second field effect transistor connected at a source to the upper power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor; and

a resistor connected between a drain of the second field effect transistor and the lower power supply.

41. The direct current sum bandgap voltage comparator of claim 40, wherein the first and second field effect transistors are p-channel MOSFETs.